Claims 1-6, 8-13 and 15-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,883,910 (hereinafter "Link") in view of U.S. Patent No. 6,037,832 (hereinafter "Kaminishi"). Applicant respectfully traverses this rejection.

A proper *prima facie* case of obviousness requires that the cited references when combined must "teach or suggest all the claim limitations," and that there be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference teachings. See Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §706.02(j).

Applicant submits that the Examiner has failed to establish a proper *prima facie* case of obviousness in the present §103(a) rejection, in that: (i) the Link and Kaminishi references, even if assumed to be combinable, fail to teach or suggest all the claim limitations; and (ii) the Examiner has failed to identify a cogent motivation for modifying the reference teachings to reach the claimed invention. Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner.

Independent claim 1 calls for a driver circuit having at least an input stage and an output stage, with the input stage being configured to include first and second differential pairs. A differential input data signal is applied to the input stage. The claim further specifies that the first differential pair has the differential input data signal applied thereto, and is implemented using MOS devices; that the second differential pair receives as its inputs corresponding outputs of the first differential pair, and is implemented using bipolar devices; and that the first and second differential pairs are configured such that application of the differential input data signal at a substantially rail-to-rail voltage swing to the first differential pair will not exceed a junction reverse bias constraint of the second differential pair.

The present invention as set forth in claim 1 thus cannot be viewed as simply an application of a general principle such as "bipolar devices and MOS devices can be substituted for one another," as alleged by the Examiner. More specifically, the claimed invention is not merely a substitution of all bipolar devices in the first and second differential pairs of the input stage of Link with MOS

devices. Instead, the claimed invention involves the specific use of MOS devices to implement the first differential pair of an input stage, and the specific use of bipolar devices to implement the second differential pair of the input stage.

This particular claimed arrangement solves an important problem associated with the all-bipolar input stage of Link, namely, that the base-emitter junction reverse bias constraint in the input stage may be violated in high-speed applications, leading to "long-term performance degradation or other types of damage for the input stage transistors" (Specification, page 1, line 23 to page 2, line 19).

The present invention as set forth in claim 1 thus provides significant advantages over the all-bipolar input stage of Link, as indicated in the following passage from page 3, lines 6-8 of the specification:

> Advantageously, the invention permits an optical source driver circuit to accommodate full differential input voltage swings, i.e., substantially rail-to-rail input voltage swings, while also maintaining the ability of the driver circuit to operate at high speeds.

As noted previously, the Examiner in formulating the §103(a) rejection of claim 1 argues that it would be obvious to modify Link so as to reached the claimed invention simply because it is well known "that bipolar devices and MOS devices can be substituted for one another," as indicated in column 18, lines 45-55. However, as noted above, the claimed invention more particularly requires that MOS devices be used to implement the first differential pair of an input stage, and bipolar devices be used to implement the second differential pair of the input stage, in a manner that solves a particular problem of the prior art. This is not simply substitution of bipolar devices for MOS devices, as in Kaminishi, because the Kaminishi teaching relied upon by the Examiner does not teach or suggest the particular mix of bipolar and MOS devices claimed. The cited portion of Kaminishi is as follows:

> The present invention can also be applied to a circuit in which all npn and pnp transistors are exchanged to reverse all current directions. Although the above embodiments have exemplified the silicon bipolar transistor, the transistor may be a GaAs- or InP-based HBT. As far as the basic circuit operation is the same, the present invention can also be applied to even another type of transistor such as a MOSFET, CMOSFET, GaAs MESFET, or HEMT except for a transistor used to obtain an output current exponentially changing with respect to an input voltage. When an FET is used in place of the bipolar transistor, the gate, drain, and source of the FET respectively replace the base, collector, and emitter of the bipolar transistor.

This passage, at best, provides a general teaching to replace bipolar transistors with MOS devices. Application of this teaching to the input stage of Link would therefore suggest to one skilled in the art that the first and second differential pairs of the Link input stage should both be implemented using MOS devices in place of bipolar devices. The proposed combination of Link and Kaminishi therefore clearly fails to meet the limitations of claim 1 relating to the use of MOS devices to implement the first differential pair of an input stage, and the use of bipolar devices to implement the second differential pair of the input stage.

Independent claim 1 thus includes limitations which are not taught or suggested by the proposed combination of Link and Kaminishi. The combined teachings of these references therefore fail to "teach or suggest all the claim limitations" as would be required by a proper §103(a) rejection.

Also, as indicated previously, the Examiner has failed to identify a cogent motivation for modifying the reference teachings to reach the claimed invention.

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual question of motivation,

which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344.

There has been no showing in the present §103(a) rejection of objective evidence of record that would motivate one skilled in the art to combine Link and Kaminishi to produce an arrangement in which MOS devices are used to implement the first differential pair of an input stage, and bipolar devices are used to implement the second differential pair of the input stage. Instead, the Examiner relies on a conclusory statement to the effect that "bipolar devices and MOS devices can be substituted for one another," which fails to address the particular mix of bipolar and MOS devices that is claimed.

Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner. More specifically, as indicated above, the teachings in column 18, lines 45-55 of Kaminishi if applied to the input stage of Link would suggest not the claimed arrangement, but instead an arrangement in which both of the first and second differential pairs of the Link input stage are implemented using MOS devices in place of bipolar devices. This is an explicit teaching away from the claimed invention, in which MOS devices are used to implement the first differential pair of an input stage, and bipolar devices are used to implement the second differential pair of the input stage, in a manner that solves a problem of the prior art.

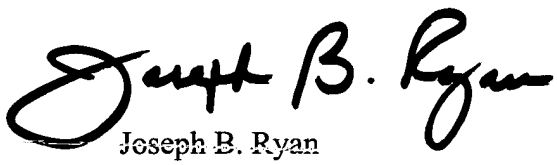
Applicant therefore respectfully submits that independent claim 1 is allowable over Link, Kaminishi and the other art of record.

Independent claims 8, 15 and 16 include input stage limitations similar to those described above with regard to claim 1, and are therefore believed allowable for substantially the same reasons identified above.

Dependent claims 2-7, 9-14, 17 and 18 are believed allowable for at least the reasons identified above with regard to their respective independent claims. The Kaminishi '481 reference fails to supplement the above-described fundamental deficiencies of Link and Kaminishi '832, and the corresponding §103(a) rejection of claims 7 and 14 is therefore traversed.

In view of the above, Applicant believes that claims 1-18 are in condition for allowance, and respectfully requests withdrawal of the §103(a) rejections.

Respectfully submitted,



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